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Admittance and Impedance Spectroscopy on Cu(In,Ga)Se_2 Solar Cells

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Abstract

The present work reports some experimental results on the electrical properties of high efficiency ZnO/CdS/Cu(In,Ga)Se_2 heterojunction solar cells. Admittance spectroscopy has been employed for characterisation of the bulk and interface levels in the absorber Cu(In,Ga)Se_2 layer. The temperature dependent capacitance-frequency analysis indicated an emission from a shallow acceptor like defect level with an activation energy of about 75 meV. Information on the equivalent circuit model of the devices has been provided by the analysis of impedance measurements. The impedance data are presented in the Nyquist plot at several dc bias voltages at 300 K. The equivalent circuit model consisting of a parallel resistor and capacitor in series with a resistor is found to give a good fit to the experimental data.

Key Words: CIGS, Solar cell, Admittance spectroscopy, Impedance spectroscopy and Equivalent circuit.

1. Introduction

Within the family of Cu-chalcopyrite semiconductors, Cu(In,Ga)Se_2 is of considerable interest for photovoltaic applications because of its desirable direct band gap in the range 1.0–1.4 eV, high optical absorption coefficient [1], a moderate surface recombination velocity and radiation resistance [2]. These properties give an opportunity for the fabrication of low cost, stable and high efficiency thin film solar cells. On the basis of Cu-III-VI chalcopyrite solar cells, conversion efficiencies above 18% have already been obtained at the research and development (R& D) level [3,4]. The electrical behaviour and the performances of Cu(In,Ga)Se_2 (CIGS) based thin film solar cells seems to be influenced mainly by the defect levels located at the CdS/CIGS interface and in the bulk of the depletion region. Thus, in order to improve device properties of these heterojunction solar cells, the characterisation of these levels is necessary. Several techniques such as Admittance spectroscopy (AS) [5-9] and deep level transient spectroscopy (DLTS) [10,11] have been applied successfully to identify these defects in Cu(In, Ga)Se_2 thin films. Despite the progress that has been made in understanding the nature of defect states in this device structure during recent years, there remain a lot of features that have not yet been explained satisfactorily. Complex impedance spectroscopy (IS) is also a well-known and powerful technique for investigating the ac behaviour dielectric materials [12]. However, it has not yet been fully utilised in the case of heterojunction devices [13].

In this work we investigate the defect structure and the equivalent circuit of polycrystalline CIGS solar cells by admittance and impedance measurements. The devices were prepared at the Institute of Physical

Electronics (IPE) of the University of Stuttgart. The small area (0.5 cm^2) Al:ZnO/CdS/Cu(In,Ga)Se_2/Mo/Glass solar cells were fabricated with the method of co-evaporation . The typical device has conversion efficiency of about 13% and Ga content of the absorber layer is Ga/(In+Ga)=0.27 as determined by energy dispersive spectroscopy.

2. Experimental Technique

The details of the preparation techniques used in the fabrication of CIGS solar cells are available elsewhere [14]. The preparation of the devices starts with the deposition of Mo thin layer on the soda-lime glass substrate by electron-beam evaporation technique. This layer acts as ohmic back contact. Absorber Cu(In,Ga)Se_2layer of about 2 μm is deposited by simultaneous evaporation of the elements in high vacuum onto Mo coated substrates heated to about 600 °C. Buffer CdS layer (≈0.01 μm) and window ZnO layer (≈500 nm) are then successively deposited by chemical bath deposition and RF sputtering techniques respectively.

All of the temperature dependent electrical measurements are carried out in the dark and in an evacuated closed-cycle helium cryostat (Oxford) equipped with a sample holder which is heated in the temperature range of 100–330 K. The AS and IS measurements are performed using a Hewlett Packard HP 4192A impedance analyser operating at frequencies 5 Hz to 13 MHz. The temperature dependent capacitance C and conductance G vs frequency f measurements are performed at zero bias and the amplitude of the ac signal is held constant at 20 mV.

3. Results and discussions

3.1. Admittance spectroscopy

It is known that admittance spectroscopy investigates the capacitance of a rectifying junction as a function of the frequency and temperature. The junction capacitance is given by the depletion layer capacitance as

$$C_{Dep} = \frac{\varepsilon_r}{w} = \left(\frac{\varepsilon_r q N_A}{2V_{bi}}\right)^{1/2} \tag{1}$$

where w is the depletion layer width, q the elementary charge, ε_r the semiconductor's dielectric constant, N_A the acceptor concentration, and V_{bi} the built-in voltage. The electronically active traps in the depletion region of the rectifying junction make contribution to the capacitance spectrum at lower frequencies and/or high temperatures. The effect of a single majority carrier trap to the junction capacitance is [15]

$$C\left(\omega\right) = C_{Dep} + \frac{C_{Lf} - C_{Dep}}{1 + \omega^2 \tau^{*2}} \tag{2}$$

where C_{Lf} is the low frequency capacitance which depends on the trap density N_T and the acceptor concentration N_A if depletion layer is in the p-type material. The τ^* is the time constant of a trap level and depends on the N_T, N_A and depletion layer width. In the case of small trap concentration, $N_T << N_A$, the time constant becomes $\tau^* = 1/\omega_o$ [16]. The inflection frequency ω_0 is related to the emission rate e_T in the limit of small trap concentrations according to,

$$\omega_0(T) = 2e_T(T) = 2N_{C,V} v_{th} \sigma_{n,p} \exp(-E_a/kT) = 2\xi_0 T^2 \exp(-E_a/kT), \tag{3}$$

where $\sigma_{n,p}$ is the capture crossection for electrons and holes, ν_{th} the thermal velocity, $N_{C,V}$ the effective density of states in the conduction and valence band and E_a is the activation energy of the defect level with

respect to the corresponding band edge. All the temperature independent parameters are included in the emission factor ξ_0. For majority carrier traps of the p-type material, the levels can be charged or discharged at frequencies lower than ω_o.

Figure 1. shows the capacitance spectra of the typical device at zero voltage bias and at temperatures between 100 and 320 K. The capacitance decreases as the frequency increases and its value increases as the temperature increases according to a thermal activation of the individual contributions of emission rates limiting to the capacitance. At a temperature between 220 K and 320 K the decrease in capacitance occurs almost at the same frequency value, indicating that the inflection frequency ω_0 does not change with temperature. However, a step-like variation is observed in the temperature range between 100 K and 200 K. This can be attributed to the frequent capture and emission of free carriers by interface states at the interface between buffer CdS and absorber CIGS layers [7,9]. The inflection frequencies in the temperature range given above were determined from maxima in the derivative -fdC/df of C(f) spectra in Figure 2. From the Arrhenius plot of $\omega_0 T^{-2}$, as shown in Figure 3, the activation energy of about E_a=75 meV and the pre-exponential factor $\xi_0 = 2.70 \times 10^3$ $s^{-1}K^{-2}$ were evaluated. Rau et al. [17,18] reported a level with comparable activation energies from admittance spectroscopy measurements and interpreted it as an shallow acceptor like defect state originated from the intentional incorporation of Na into the absorber CIGS layer.

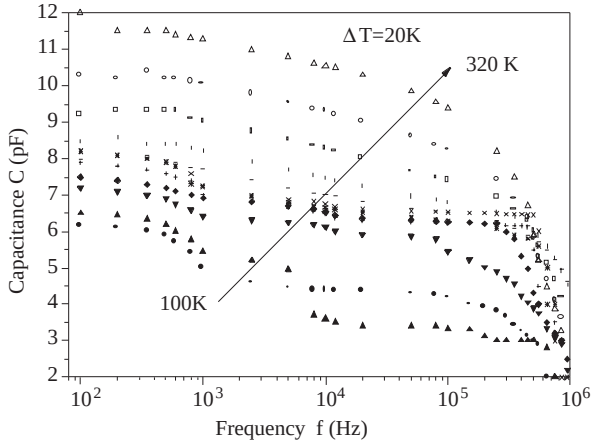

Figure 1. Capacitance – frequency curves taken at temperatures between 100 and 320 K.

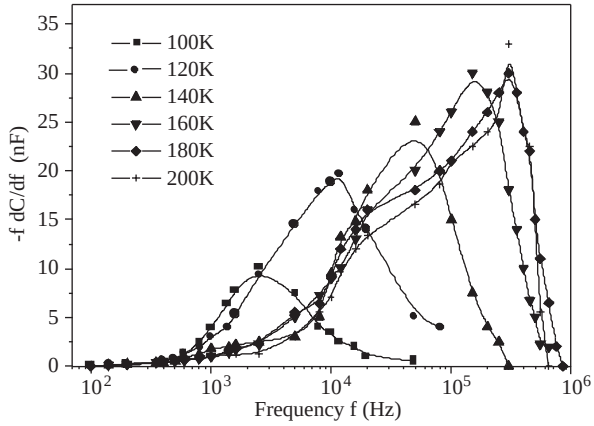

Figure 2. Differentiated spectra at temperatures between 100 and 200K.

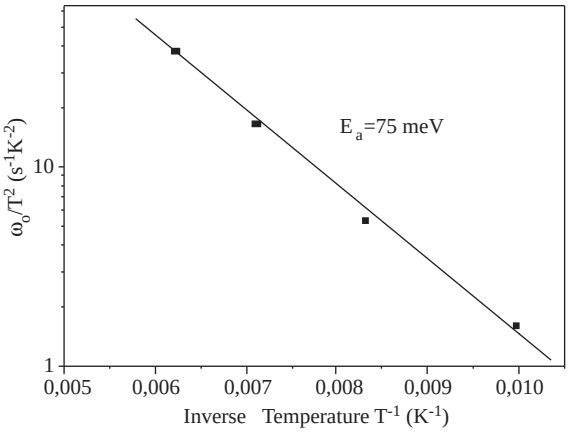

Figure 3. Arrhenius plot of the transition.

3.2. Impedance spectroscopy

AC impedance spectroscopy provides frequency resolved information which can detach the contributions of different component regions (e.g. bulk, material/contact and interface between the n and p type regions) to the total electrical properties of heterojunction devices through differences in the time constants of each element [13,19,20]. The ac equivalent circuit of a pn heterojunction solar cell consists of 3 elements: the series resistance R_s (due to bulk and contact resistances); the parallel resistance R_p (due to recombination in the depletion region) and the total capacitance C_o (sum of diffusion and depletion capacitances) [13,20]. The theoretical values of real and imaginary components of such circuit were calculated using the relationships

$$Z^{'} = R_s + \frac{R_p}{1 + \omega^2 C_o^2 R_p^2} \tag{4}$$

$$Z'' = \frac{\omega C_p R_p^2}{1 + \omega^2 C_o^2 R_p^2}. \tag{5}$$

Since the components of total capacitance are in parallel, this equivalent circuit has a single time constant $\tau = R_p C_o$ and the plot of Z' vs Z'' for a range of frequencies should be a semicircle with diameter R_p, displaced from origin by R_s [19].

Figure 4 shows the ImZ (Z') vs ReZ (Z'') plots of the typical device at several dc bias voltages at room temperature. The semicircular nature of plots indicates the predominance of a single time constant. The electrical response can be fitted by an equivalent ac circuit composed by a single parallel R_p resistor and capacitor C_o network connected with a series resistance R_s. The value of C_o ($=Y''/\omega$) was found to be slightly frequency dependent therefore it was averaged over the whole frequency range. The series resistance R_s, to the capacitor is determined from the minimum Z' value at the highest frequency. The Z' value at the lowest frequency represents the sum of the series resistance and the parallel resistance (R_s+R_p) to the capacitance. The value of the series and parallel resistance values were found in between $R_s \sim 6 - 8 \times 10^3 \Omega$ and $R_p \sim 3 - 2 \times 10^4 \Omega$ as the bias voltage decreases from +0.8 V to –0.8 V respectively. Since the resistances of the Mo back contact and the bulk of ZnO layer are negligible, the physical origin of this relatively high series resistance may possibly be due to the bulk resistivity of CIGS layer [21]. The slight decrease in parallel resistance with voltage may be due to the leakage paths which can physically due to generation-recombination currents within the depletion region [22]. The solid lines representing the fitting results using the corresponding equivalent circuit, as drown in Figure 4, are shown to be well fitted except in the low frequency range. AS of CIGS solar cells prepared under similar conditions with ratio Ga/(Ga+In) < 0.3 has

been indicated that the interface states has important contribution to the electrical properties of this devices [23]. Therefore, it may well be possible that the slight departure of Z' vs Z'' plot from the ideal behaviour observed in the low frequency range is a matter of the interface states located at CdS/CIGS junction rather than additional capacitive effects due to ohmic contact-CIGS interface.

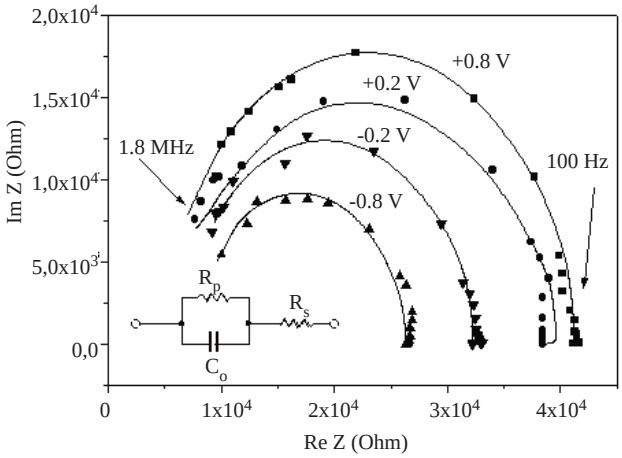

Figure 4. The Nyquist plots of the typical device (symbols) and their fit with an equivalent ac circuit (solid line) at ±0.8 and ±0.2 dc bias voltages.

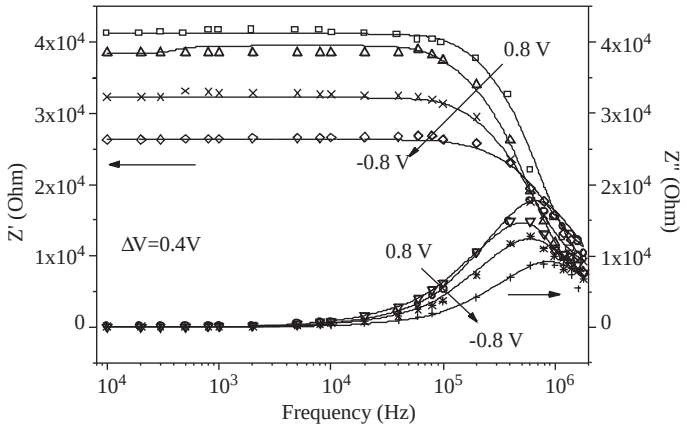

Figure 5. The frequency dependent real and imaginary part of the impedance spectrums (symbols) and their fit with an equivalent ac circuit (solid line) at ±0.8 and ±0.2 dc bias voltages.

The frequency dependent theoretical and measured real and imaginary parts of the impedance spectrums at ±0.8 and ±0.2 dc bias voltages are plotted in Figure 5. The solid lines representing the fitting results using the corresponding equivalent circuit, are shown to be well-fitted over the frequency range studied. The absence of more than one semicircle certainly signifies the effect of any other capacitive components,which may originate from the electrode-semiconductor interface in this device structure.

4. Conclusion

We have investigated the interfacial properties of the ZnO/CdS/Cu(In,Ga)Se_2 solar cells by admittance and impedance spectroscopy carried out in the frequency range 100 Hz –1.8 MHz. A Na related shallow trap level at E_V+0.075 eV in the absorber layer was found by admittance measurements. The ac impedance

data were measured at room temperature for voltages ranging from +0.8 V to –0.8 V. The observation of semicircular behaviour in the Nyquist plots imply that the observed dielectric response can be described by an equivalent circuit consisting of a parallel resistor R_p and capacitor C_o in series with a resistor R_s. There are no other capacitive components which may originate due to the electrode-semiconductor interface in this device structure. This was checked with the frequency dependency of both the imaginary and the real part of the impedance data and found that the same equivalent circuit model applies. The experimental data have also indicated the existence of interface states at CdS/CIGS and/or in CIGS as expected for this device structure.

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